Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-8 (Canceled)

Claim 9 (Currently amended): A method ~~of arranging plural circuits,~~ comprising:

a) arranging a plurality of substantially similar signal processing circuits together in a predefined pattern so that a signal transfer delay time between each ~~said~~ signal processing circuit in the plurality of signal processing circuits is substantially the same; and

b) providing in ones of said plurality of signal processing circuits:

one or more signal processing circuits for receiving a plurality of data signals~~, and~~;

one or more circuits for processing ~~the~~ the plurality of data signals according to an algorithm~~,~~; and

one or more circuits for receiving the plurality of data signals from an input and for transferring the input data signals to other signal processing circuits for processing therein.

Claim 10 (Currently amended): The method of ~~Claim~~ claim 9, wherein said plurality of signal processing circuits comprise a plurality of data processors.

Claim 11 (Currently amended): The method of ~~Claim~~ claim 10, wherein ones of said data processors process the data signals according to different algorithms.

Claim 12 (Currently amended): The method of ~~Claim~~ claim 9, wherein each signal processing circuit in said plurality of signal processing circuits transfers data signals only to ~~neighbor~~ neighboring signal processing ~~circuit~~ circuits in said plurality of signal processing circuits.

Claim 13 (Currently amended): The method of ~~Claim~~ claim 9, further including arranging said plurality of signal processing circuits in a plane.

Claim 14 (Currently amended): The method of ~~Claim~~ claim 9, further including arranging said plurality of signal processing in ~~plural~~ a plurality of planes, where ~~the~~ a signal transfer delay between planes in the plurality of planes is substantially the same as between signal processing circuits in the same plane.

Claims 15 - 19 (Canceled)

Claim 20 (New): A system, comprising:

(a) at least one interfacing module for digitizing a multi-channel data stream into a plurality of multi-channel data sets, wherein

each multi-channel data set in the plurality of multi-channel data sets represents a discrete time interval;

each multi-channel data set in the plurality of multi-channel data sets comprises a plurality of data signals;

said at least one interfacing module is configured to assign a time stamp to each data signal in each multi-channel data set; and

said at least one interfacing module is configured to determine a property, other than said time stamp, of each data signal in each multi-channel data set;

(b) a processor complex in electrical communication with said at least one interfacing module such that said processor complex receives ones of said multi-channel data sets in said plurality of multi-channel data sets from said at least one interfacing module at said discrete time interval, the processor complex comprising a plurality of channels, each channel in said plurality of channels adapted to receive one or more signals in said multi-channel data set, each channel comprising:

at least a first processor and a second processor; wherein

said first processor and said second processor each respectively have an input port and an output port;

said first processor is associated with a bypass switch and a bypass register, said bypass switch having (i) a first state that causes a signal in said multi-channel data set to bypass said first processor and be stored in said bypass register and (ii) a second

state that causes a signal in said multi-channel data set to be input into said first processor; and

the input port of the second processor is adapted to receive data corresponding to one of said plurality of signals from the output port of the first processor; and

(c) at least one decision module adapted to receive and analyze processed data from all or a portion of the channels in said plurality of channels.

Claim 21 (New): The system of claim 20, wherein each of said first and second processors includes at least one bi-directional port communicating with corresponding first and second processors of neighboring channels in said plurality of channels.

Claim 22 (New): The system of claim 20, further comprising:

a first chip in electrical communication with said interfacing module and including a plurality of said first processors; and

a second chip in electrical communication with said first chip and including a plurality of said second processors,

wherein said first chip and said second chip are arranged on a substrate configured to permit digital signals processed by each channel in the plurality of channels to flow from said first chip to said second chip.

Claim 23 (New): The system of claim 22, wherein the substrate comprises a printed circuit board that includes the interfacing module.

Claim 24 (New): The system of claim 22, further comprising at least one crate in communication with the decision module, wherein each crate in said at least one crate includes a plurality of printed circuit boards and wherein each printed circuit board in the plurality of printed circuit boards includes said first chip and said second chip arranged to permit signals in the plurality of signals processed by each channel in the plurality of channels to flow from said first chip to said second chip.

Claim 25 (New): The system of claim 22, wherein said first chip includes at least sixteen of said first processors and said second chip includes at least sixteen of said second processors.

Claim 26 (New): The system of claim 20, wherein each processor in said plurality of channels is constructed substantially identically.

Claim 27 (New): The system of claim 20, wherein each of said plurality of channels includes n number of processors, including said first processor and said second processor, wherein n is greater than two.

Claim 28 (New): The system of claim 27, wherein n is at least ten.

Claim 29 (New): The system of claim 20, wherein, for each respective channel in said plurality of channels, a processor in said respective channel is programmable so that a desired number of data bits can be input and processed, and another desired number of raw data bits can be passed to a subsequent processor in the respective channel.

Claim 30 (New): The system of claim 20, further comprising a processor stack comprising said plurality of channels, wherein the input to each channel in the plurality of channels receives data corresponding to a different portion of said multi-channel data set in each said multi-channel data set in said plurality of multi-channel data sets, and wherein each processor of said stack is programmable so as to be data driven as a function of receipt of a multi-channel data set in said plurality of multi-channel data sets.

Claim 31 (New): The system of claim 30, wherein the stack comprises a first processing layer and a second processing layer, wherein

the first processing layer comprises said first processor of each channel in said plurality of channels; and

the second processing layer comprises said second processor of each channel in said plurality of channels, and wherein

each of said first processors includes a bi-directional port for communicating with a neighboring processor in said first layer; and

each of said second processors includes a bi-directional port for communicating with a neighboring processor in said second layer.

Claim 32 (New): The system of claim 31, further comprising a plurality of processing layers comprising a multi-layer stack, the multi-layer stack including said first processing layer and said second processor layer, and wherein a number of processor layers of said multi-layer stack is a function of an amount of time required for a processor in said multi-layer stack to complete a predetermined algorithm.

Claim 33 (New): The system of claim 32, further comprising a plurality of cards in electrical communication with a printed circuit board, wherein each card comprises a plurality of processors corresponding to one of said processing layers of said multi-layer processing stack.

Claim 34 (New): The system of claim 33, wherein one or more cards in said plurality of cards represent said first processing layer.

Claim 35 (New): The system of claim 33, further comprising at least one crate in communication with said decision module, each crate including a plurality of said printed circuit boards.

Claim 36 (New): The system of claim 20, wherein said

the first processor is configured to execute a non-interruptable real-time algorithm on one or more data signals in each multi-channel data set;

the data stream is delivered to said system at a data rate of tens of MHz or higher; and

said discrete time interval is less than a time in which a said first processor completes an instance of said non-interruptable real-time algorithm on one or more signals in a multi-channel data set in said plurality of multi-channel data sets.

Claim 37 (New): The system of claim 20, further comprising a data collection pyramid having a plurality of inputs for receiving data from each of said channels and adapted to route data corresponding to an event of interest to said decision module.

Claim 38 (New): The system of claim 20, wherein an interfacing module in the at least one interfacing module comprises:

instructions for synchronizing said plurality of signals; and

instructions for delivering data corresponding to said plurality of signals to one or more channels in said plurality of channels.

Claim 39 (New): An apparatus for processing, in real-time, a multi-channel data set arriving at a data rate of tens of MHz or higher, and for providing a computational result within a few hundreds of nanoseconds from a time when the multi-channel data set arrived at said apparatus, the apparatus comprising:

(a) at least one interfacing module for conditioning a plurality of received signals in said multi-channel data set, wherein each received signal in the plurality of received signals corresponds to a channel in said multi-channel data set; and wherein the at least one interfacing module collectively comprises:

instructions for assigning a time stamp to each received signal in said plurality of received signals, each said time stamp corresponding to a time when the corresponding received signal in the plurality of received signals was generated or detected;

instructions for determining a property, other than a time stamp, of each received signal in the plurality of received signals; and

instructions for converting the property and the time stamp for each received signal in the plurality of received signals to a corresponding digital signal, thereby forming a plurality of digital signals;

(b) a plurality of processor channels, the plurality of processor channels arranged so that logical or actual neighboring processor channels represent digital signals derived from neighboring received signals in said multi-channel data set, the plurality of processor channels adapted to receive and process the plurality of digital signals, each processor channel in the plurality of processor channels comprising a processor having a capability of signal correlation between neighboring processor channels in said plurality of processor channels; and

(c) at least one decision module adapted to receive and analyze processed data from each processor channel in said plurality of processor channels, the at least one decision module configured to analyze data from said plurality of processor channels based at least on said time-stamp and said property in each digital signal in said plurality of digital signals so that data from said plurality of processor channels can be correlated irrespective of whether such data was processed by neighboring processor channels in said plurality of processor channels to thereby determine whether a pattern of interest occurs in said data set.

Claim 40 (New): The apparatus of claim 39 wherein the property is an amplitude, area, charge, or voltage associated with said received signal.